For PTO-1449 (Modified)	U.S. Department of Commerce Patent and Trademark Office	Atty. Docket No. 30320/14617A	Serial No. 10/728,404
INFORMATION DISCLOSURE STATEMENT		Applicant: Doros, Theodore G.	
		Filing Date: December 5, 2003	Group: ~~2875~~ 2883

U.S. PATENT DOCUMENTS							
*Examiner Initials		Document Number	Issue Date	Name	Class	Subclass	Filing Date if Appropriate
cmc		5361292	11-1-94	Sweatt	378	34	
cmc		5638211	6-10-97	Shiraishi	359	559	
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cmc		6452662	9-17-02	Mulkens et al.	355	67	4-6-99
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OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)		
cmc		Sewell, "The Development of Step and Scan," Semiconductor Fabtech, 9th Edition, pp. 193-197
cmc		Schellenberg et al., "Adoption of OPC and the Impact on Design and Layout," Session 7-4, Design Automation Conference, June 19, 2001
cmc		Rieger et al., "Layout Design Methodologies for Sub-Wavelength Manufacturing," Website, 20 pages, (undated), found at: http://videos.dac.com/videos/38th/7/7_3/7_3 slides.pdf
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cmc		Hsu et al., "Dipole Decomposition Mask-design for Full Chip Implementation at the 100nm Technology Node and Beyond," Optical Microlithography XV, Proceedings of SPIE, Vol. 4691, © 2002, pp. 476-490

Examiner: Chris Kalwood	Date Considered: August 10, 2004

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.